University of Computer Studies, Yangon
B.C.Sc./B.C.Tech.

CT-305	**:**	**Computer Architecture I**	**Second Semester**
Text book	**:**	Computer Architecture and Organization (3rd Edition) by John P. Hayes	
Period	**:**	45 periods for 15 weeks (3 periods/week) (Lecture + Lab)	

CT 305 Computer Architecture and Organization

Course Description

Basic hardware and software concepts in the analysis and design of embedded systems. This course discusses the basic structure of a digital computer and used for understanding the organization of various units such as Control unit, Arithmetic and Logical unit, Memory unit and I/O unit in a digital computer.

Course Objectives

- To have a thorough understanding of the basic structure and operation of a digital computer.
- To understand the operation of the arithmetic unit including the algorithms & Implementation of Fixed-point and floating-point arithmetic operations.
- To learn the concepts behind advanced pipelining, vector processing techniques and control unit designs.
- To understand the current state of art in memory system design.
- To study the different ways of communicating with I/O devices and standard I/O interfaces.

Assessment Plan for the Course

Paper Exam: 60%

Attendance: 10%

Test/ Quiz: 10%

Lab: 10%

Lab Assessment: 10%

Tentative Lecture Plan

No.	Chapter	Page	Period	Figures, Examples and Problems
	Chapter 1 Computing and Computers	1-63	**4**	General Knowledge
1.	1.1 The Nature of Computing 1.2 The Evolution of Computers	1-35	2	Fig. 1.1 to 1.15, 1.17 Eg. 1.1,1.3 to 1.5 Prob. 1.1 to 1.4, 1.11, 1.12
2.	1.3 The VLSI Era	35-57	2	Fig. 1.18, 1.19, 1.22 to 1.31 Eg. 1.7 Prob.1.28,1.29,1.33, 1.34, 1.35
	Chapter 2 Design Methodology	64-136	**20**	
3.	2.1 System Design 2.1.1 System Representation 2.1.2 Design Process	64-73	3	Fig. 2.1 to 2.8 Eg. 2.1 Prob. 2.1 to 2.4
4.	2.1.3 The Gate Level	73-83	4	Fig. 2.9 to 2.14 Eg. 2.2 Prob. 2.7 to 2.12, 2.16 to 2.17
5.	2.2 The Register Level 2.2.1 Register-level Components Multiplexer Decoders Encoder	83-91	3	Fig. 2.15 to 2.25 Eg. 2.3 Prob. 2.19, 2.20, 2.21,2.23
6.	Arithmetic elements Register Counter	91-97	3	Fig. 2.26 to 2.31 Eg. 2.4 Prob. 2.24 to 2.26,

No.	Chapter	Page	Period	Figures, Examples and Problems
	Buses			2.28, 2.29, 2.39, 2.40, 2.41, 2.42
7.	2.2.2 Programmable Logic Devices 2.2.3 Register - Level Design	97-114	3	Fig. 2.32 to 2.44 Eg. 2.5, 2.6, 2.7 Prob. 2.30, 2.32, 2.33,2.36, 2.38, 2.42
8.	2.3 The Processor Level 2.3.1 Processor Level Components 2.3.2 Processor Level Design Queuing Models	114-127	4	Fig. 2.45 to 2.53 Eg. 2.8 Prob. 2.43 to 2.47 2.50 to 2.52
	Chapter 3 Processor Basics	137-222	**19**	
9.	3.1 CPU Organization 3.1.1 Fundamentals	137-147	2	Fig. 3.1 to 3.6 Eg. 3.1 Prob. 3.1 to 3.3
10.	3.1.2 Additional Features Architecture extensions Pipelining	147-154	2	Fig. 3.7 to 3.10 Eg. 3.2, Prob. 3.4 to 3.9
11.	A CISC Machine Coprocessors Other design features	154-160	3	Fig. 3.11 to 3.14 Eg. 3.3 Prob. 3.10 , 3.11, 3.13, 3.14
12.	3.2 Data Representation 3.2.1 Basic Formats	160-166	2	Fig. 3.15 to 3.20
13.	3.2.2 Fixed-Point Numbers 3.2.3 Floating Point Numbers	166-178	5	Fig. 3.21 to 3.26 Eg. 3.4 Prob. 3.26 to 3.30
14.	3.3 Instruction Sets 3.3.1 Instruction Formats	178-191	3	Fig. 3.27 to 3.31 Eg. 3.5,3.6 Prob. 3.33, 3.35, 3.37
15.	3.3.2 Instruction Types 3.3.3 Programming Considerations	191-212	2	Fig. 3.32 to 3.40 Eg. 3.7,3.8 Prob. 3.40, 3.41,3.45, 3.49
16.	Revision		**2**	All Chapters

No.	Lab	Period	Description

	Very High Speed Integrated Circuit Hardware Description Language (VHDL)	**15**	**ModelSim Simulator Software**
1.	Lab 1	1	VHDL Introduction with ModelSim Simulator Software
2.	Lab 2	1	Logic gates with VHDL
3.	Lab 3	1	Half adder, Full adder (Structureal and behavioral description)
4	Lab 4	1	Half subtractor, Full subtractor (Structureal and behavioral description)
5.	Lab 5	1	Multiplier
6.	Lab 6	1	Decoders, Encoders
7.	Lab 7	1	Multiplexer, Demultiplexer
8.	Discussion / Lab review	1	
9.	Lab Assessment 1	1	
10.	Lab 8	1	Flip flop(D, JK)
11.	Lab 9	1	Registers(Left Shift, Right Shift, Left Rotate, Right Rotate)
12.	Lab 10	2	Counters
13.	Discussion / Lab review	1	
14.	Lab Assessment 2	1	

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Attendance: 10%

Test/ Quiz: 10%

Lab: 10%

Lab Assessment: 10%